



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,178	10/16/2003	Jaw-Jung Shin	TS02-776	9069

47390 7590 12/11/2006

THOMAS, KAYDEN, HOSTEMEYER & RISLEY LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER

ROSASCO, STEPHEN D

ART UNIT PAPER NUMBER

1756

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/687,178	Applicant(s) SHIN ET AL.	
	Examiner Stephen Rosasco	Art Unit 1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-23 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>1/15/04</u> . | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Applicant's election without traverse of Group I (claims 1-23) in the reply filed on 9/7/06 is acknowledged.

Claims 2-23 are indicated as Allowable.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (7,014,956) in view of Toublan et al. (6,807,662).

The claimed invention is directed to a method is provided for reducing Critical Dimension (CD) non-uniformity in creating a patterned layer of semiconductor material. Two masking layers are respectively created, the first masking layer comprising a main pattern, an isolated pattern and a dummy pattern, the second masking layer exposing the dummy pattern. Methods of compensating for optical proximity effects and micro-loading, as provided by the invention, are applied in creating the first masking layer. The patterned first masking layer is transposed to an underlying layer creating a first pattern therein. The second masking layer removes the dummy features from the transposed first pattern, creating a second pattern therein comprising a main pattern and an isolated pattern to which compensation for optical proximity effects and micro-loading have been applied.

Chen et al. teach a set of masks comprising: a first mask having a first low transmittance region to transmit comparatively low intensity radiation to a radiation

sensitive layer and a first high transmittance region to transmit comparatively high intensity radiation to the radiation sensitive layer; and a second mask having a second high transmittance region that corresponds to the first low transmittance region and a second low transmittance region that corresponds to the first high transmittance region.

And further comprising a portion of the first mask to expose a feature in the radiation sensitive layer; and a radiation intensity reducer of the second mask to reduce a subwavelength distortion of the feature.

The teachings of Chen et al. differ from those of the applicant in that the applicant teaches that the second masking layer removes the dummy features from the transposed first pattern, creating a second pattern therein comprising a main pattern and an isolated pattern to which compensation for optical proximity effects and micro-loading have been applied.

Toublan et al. teach a set of masks with definitions created by reading at least a portion of an initial layout of an integrated device layer, identifying one or more target features within the initial layout, creating a first revised layout definition for a first mask, the first revised layout definition including the one or more target features and adjacent clear areas inside dark-field content, and creating a second revised layout definition for a second mask, the second revised layout definition including one or more dark features inside bright-field content, wherein the one or more dark features, when used in a multiple exposure fabrication process, will overlap the one or more target features.

Toublan et al. also teach (col. 8, lines 39-50) FIGS. 7D-7G illustrate the creation of layouts for masks with assist features, according to one embodiment of the present invention. FIGS. 7D and 7E illustrate the creation of layouts for the first and second masks

Art Unit: 1756

when distance $d_{sub.ap}$ between the active region and the poly region exceeds a certain threshold (e.g., 0.16 μm). In FIG. 7D, the assist feature is narrow enough as not to be printable on the wafer. In FIG. 7E, the assist feature is printable on the wafer.

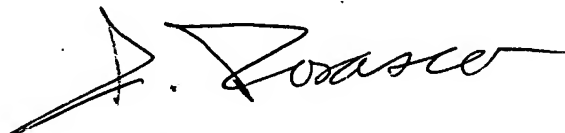
Accordingly, the layout for the second mask includes a clear area to cause removal of the resulting scatter bar from the wafer. The clear area in the second mask may be extend beyond the assist feature by a parameter nS on each side.

It would have been obvious to one having ordinary skill in the art to take the teachings of Chen et al. and combine them with the teachings of Toublan et al. in order to make the claimed invention because Toublan et al. teach removing the scattering bar which is known to be used to reduce a subwavelength feature distortion.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco
Primary Examiner
Art Unit 1756

S. Rosasco
12/5/06